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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/322,321	05/28/1999	TONIA MORRIS	042390.P6888	7825

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EXAMINER

GENCO, BRIAN C

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/322,321	Applicant(s) MORRIS ET AL.	
	Examiner Brian C Genco	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 23-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

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Applicant's amendment filed June 8, 2004 has been fully considered by the Examiner but is not deemed persuasive.

Applicant argues that the limitation of claim 1 reciting "integration time for first color and second color can be set independently by using the control logic to control timing of the first reset bit fed to each of the first and second reset shift registers" is not disclosed since Suzuki teaches away from this limitation by teaching to reset all colors with the first reset bit at the same time and to then vary the integration time of the colors by reading them out at different times.

In response, Examiner notes that the Suzuki reference does not teach away from the claim limitations in that the disclosure of Suzuki in column 4, lines 27-41 discloses an embodiment wherein Suzuki provides a readout register for each color so as to enable concurrent readout of each color at some time period. Thus, while Suzuki does not explicitly disclose that start time of the various colors are staggered and the end time occurs at the same time Suzuki does implicitly teach this limitation through a circuit structure that is capable of this.

Examiner asserts that the claim limitation and the disclosure in Fig. 3 of the Suzuki reference are functional equivalents of each other. Evidence of this functional equivalence is found in the previously relied upon USPN 5,541,645 to Davis in Fig. 4C. Examiner notes the functional equivalence to providing the starting reset bit to all colors at and to then provide the second reset bit at staggered times so as to vary the integration time of each color as shown in Fig. 3 of Suzuki to the staggering of the starting reset bit

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for the various colors so as to vary their integration time and then providing the second reset bit simultaneously to all the colors as disclosed by Davis in Fig. 4C.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 25 and 31-35 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for providing two metal lines for each row, does not reasonably provide enablement for providing less than two metal lines for each row. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. Examiner notes that there is no disclosure of having a color filter pattern wherein only one color is on each row. As such, there is no enablement for less than two metal lines for each row. Claims 32-35 depend on claim 31.

Claims 33-35 rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for providing two of the reset shift registers with a pair of reset signals, does not reasonably provide enablement for providing the third reset shift register with a pair of reset signals. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. As shown in Fig. 4 the blue color channel only has one reset bit. As such there is no enablement for providing each of the first, second, and third, reset shift registers with a pair of reset bits. Examiner suggests

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claiming that the control logic feeds two of the reset shift registers with a pair of reset signals. Claims 34 and 35 depend on claim 33.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 23, 24, and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,609,825 to Berger et al.) in view of (US PG-PUB 2003/0193597 to Fossum et al.) in further view of (USPN 4,709,259 to Suzuki) in view of (USPN 5,541,645 to Davis).

In regards to claim 23 Berger et al., herein Berger discloses an integrated circuit comprising:

a pixel array (e.g., see Fig. 1);

a first reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements that are in a respective one of the rows of the array (e.g., element 4 of Fig. 1);

a wordline shift register having a plurality of outputs, each output being coupled to control a readout of the sensor elements that are in a respective one of the rows of the array (e.g., element 5 of Fig. 1);

control logic coupled to feed (a) the first shift register with a reset bit and (b) the wordline shift register with a read bit, and to operate the reset and wordline shift registers so that the reset bit and the read bit shift through their respective registers while an image frame is being captured, with the reset bit always being one or more rows ahead of the

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read bit to mark the start of integration, wherein the control logic is to program the reset bit and the read bit to set the integration time independently for different lines (e.g., column 4, lines 24-30 and 52-60; column 5, lines 14-27; Fig. 2).

Berger does not disclose that the reset bit is used for generating a correlated double sampling (CDS) reset value. In contrast, Berger discloses draining the reset charges (column 4, lines 24-30 and 52-60). It is extremely well known in the art to use the reset bit in order to generate a CDS reset value as taught by Fossum et al. Fossum et al., herein Fossum, discloses sampling a reset voltage at the end of integration in order to reduce various noise introduced into the signals (paragraphs 0028, 0029, and 0033).

Neither Berger nor Fossum disclose a color sensor array having a plurality of sensor elements of different first and second colors, arranged in rows and columns, wherein the first reset shift register is used to control the integration time of the first color and a second reset shift register is used to control the integration time of the second color.

Suzuki discloses a color image sensor wherein the integration time for each color is adjustable so as to increase the dynamic range of the sensor (column 2, lines 17-21). This is accomplished by having separate registers for each color so as to reset all of the colors at the same time to start the integration period and to read out the colors at their respective integration times as depicted in Fig. 3 (e.g., column 4, lines 6-41; column 5, line 27 – column 6, line 16); Figs. 1-3). Therefore it would have been obvious to have had separate reset shift registers for each color so as to enable variable exposure times not only on different lines but on different colors as well thereby increasing the dynamic range of the sensor. As such, for at least the red and green colors two reset bits would be

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needed, one to mark the start of integration as taught by both Berger and Suzuki and the other to perform CDS at the end of the integration period as taught by Fossum.

Examiner notes that Suzuki discloses to set the integration time for each color independently by using the second reset bit. Examiner asserts that utilizing the second reset bit to vary the integration time as disclosed by Suzuki in Fig. 3 is functionally equivalent to utilizing the first reset bit to vary the integration time. Evidence of this functional equivalence is found in the previously relied upon USPN 5,541,645 to Davis in Fig. 4C. Examiner notes the functional equivalence to providing the starting reset bit to all colors at and to then provide the second reset bit at staggered times so as to vary the integration time of each color as shown in Fig. 3 of Suzuki to the staggering of the starting reset bit for the various colors so as to vary their integration time and then providing the second reset bit simultaneously to all the colors as disclosed by Fig. 4C of Davis. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have varied the integration time of the colors with the first reset bit instead of the second reset bit since they are functional equivalents of each other. Further, Examiner notes that the disclosure of Suzuki implicitly discloses the limitation of utilizing the first reset bit to vary the integration time through the provision of the circuit structure illustrated in Fig. 2 and the disclosure of column 4, lines 27-41.

In regards to claim 24 see Fig. 1 of Suzuki.

In regards to claim 26 see Examiners notes on the rejections above. Examiner notes that it is known in the art that in conventional lighting the blue color typically has the lowest intensity thus has the longest integration time. Davis discloses that since this is the case, in order to have a time efficient image sensor, and minimize dead time one



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would only want to reset the blue color once (e.g., column 5, line 26 – column 6, line 7).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have only had one reset for the blue reset register, or third reset register, in order to minimize dead time and thus have a time efficient image sensor.

In regards to claim 27 see examines notes on the above rejections.

In regards to claim 28 see examines notes on the above rejections.

In regards to claim 29 see examines notes on the above rejections. Note that the combined teaching of Berger and Suzuki teach to have a reset shift register for each color. Note further that Suzuki discloses using the Bayer color filter wherein all three colors are present on any one given line. As such, one of ordinary skill in the art would recognize that three reset metal lines would be used for each row. As such there are two reset metal lines for each row.

In regards to claim 30 see examines notes on the above rejections.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,609,825 to Berger et al.) in view of (US PG-PUB 2003/0193597 to Fossum et al.) in view of (USPN 4,709,259 to Suzuki) in view of (USPN 5,541,645 to Davis) in view of (USPN 3,971,065 to Bayer).

In regards to claim 25 Examiner notes that Suzuki does disclose a Bayer color filter array as shown in Fig. 1. Bayer discloses a color filter array pattern shown in Fig. 1B wherein this pattern provides for the luminance-sensitive elements to have the highest element population while providing a pattern that enables sampling of an image for all three basic color vectors to be symmetrical and uniform in two orthogonal directions

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(column 3, line 55 – column 4, line 2). Therefore it would have been obvious to have utilized the Bayer color filter array pattern shown in Fig. 1B of Bayer, wherein the luminance element Y is green, the first chrominance element C1 is red, and the second chrominance element C2 is blue, so as to provide for the luminance-sensitive elements to have the highest element population while providing a pattern that enables sampling of an image for all three basic color vectors to be symmetrical and uniform in two orthogonal directions.

As such only two colors are present on any one given line. Thus, one of ordinary skill in the art would recognize that two reset metal lines would be used for each row. Therefore, there are less than or equal to two reset metal lines for each row coupled to a respective pair of first and second registers.

Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,609,825 to Berger et al.) in view of (US PG-PUB 2003/0193597 to Fossum et al.) in view of (USPN 4,709,259 to Suzuki) in view of (USPN 3,971,065 to Bayer).

In regards to claims 31-35 see Examiners notes on the rejections above.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 703-305-7881 or by fax at 703-746-8325. The examiner can normally be reached on Monday thru Friday 8:30am to 4:30 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is 703-308-4357.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian C Genco  
Examiner  
Art Unit 2615

September 2, 2004



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